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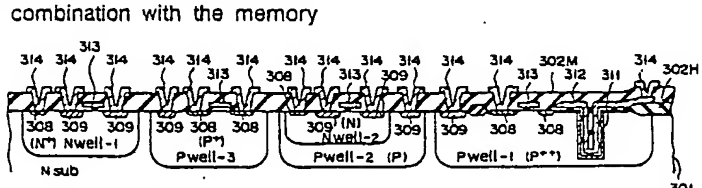
(54) Semiconductor device having different impurity concentration wells.

(57) A semiconductor device comprises an N-type semiconductor substrate (301), a first P-type well (P-well-1) formed in the semiconductor substrate (301), a second P-type well (P-well-2) formed adjacent to the first P-type well (P-well-1) in the semiconductor substrate (301), the surface impurity concentration (P) of the second P-type well (P-well-2) being set lower than that (P^{++}) of the first P-type well (P-well-1), a DRAM memory cell structure (311, 312) formed in the first P-type well (P-well-1), and an MOS transistor structure formed in the second P-type well (P-well-2) to function in combination with the memory cell structure.



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Semiconductor device having different impurity concentration wells

This invention relates to a semiconductor memory with well structure, and more particularly to a dynamic random access memory (DRAM) with CMOS structure.

In the conventional DRAM, CMOS structure has not been employed to constitute the peripheral circuit of the memory cell array. Recently, however, user of DRAMs with CMOS structure is growing.

Fig. 1 shows an example of the cross section of a one-transistor one-capacitor type DRAM with CMOS structure. In Fig. 1, 1 denotes a P-type Si body; 2 and 2*, P-wells formed in the same manufacturing step; 3, an N-well; 4, an insulation film for a capacitor; 5, a capacitor electrode; 6, the gate insulation film of a transistor; 7, the gate electrode of a transistor; 8 and 8*, N^{*}-type diffusion layers (source, drain); 9, P^{*}-type diffusion layers (source, drain); 10, an insulation film, 11, an Aℓ wiring layer; A, a memory cell section; and B, the peripheral circuit thereof. P-well layer 2 is formed to have an impurity concentration higher than that of P-type substrate 1.

Recently, it is found that it is preferable to form a memory cell in a high impurity concentration well in order to prevent a soft error.

In a conventional memory device, the impurity concentration of P-well 2* in which the memory cell is formed is the same as that of P-well 2 in which the peripheral circuit is formed. Therefore, it becomes necessary to further increase the impurity concentration of the well for the memory cell in order to suppress the soft error. From the circuit characteristic point of view, it is not desirable to excessively increase the impurity concentration of the well because it will increase the diffusion capacitance between N^{*}-type layer 8* and P-well 2* and lower the junction breakdown voltage. If the miniaturization technique of the IC internal structure is further advanced, it becomes necessary to operate the internal circuit on a voltage of 2 to 4 V, despite that input/output circuit section of the IC is operated on a voltage of 5 V. Thus, it becomes necessary to adequately change the impurity concentration of the well, such as P-wells 2 and 2*, according to the difference in the power source voltages. However, there has been developed no practical technology to meet the requirement.

An object of this invention is to provide a semiconductor device which can improve the trade-off between the soft error and the withstanding voltage by utilizing different impurity concentration wells.

One of the features of this invention is that a plurality of wells of the same conductivity type with different surface impurity concentrations are formed in the semiconductor body and a memory cell or cells are formed in that one of the wells which has the highest surface impurity concentration.

Further, this invention has a second feature that first wells of a first conductivity type (P) are formed in the semiconductor body (P or N), a first well of a second conductivity type (N) is formed in one or more wells selected from the first wells of the first conductivity type so as to form a second well or wells of the first (P) or second (N) conductivity type, and a memory cell or cells are formed in one of the wells having the highest surface impurity concentration.

Thus, the basic feature of this invention is that the second conductivity type well is formed in one or more selected wells of the first conductivity type in order to partly neutralize the first conductivity type impurity (P) with the second conductivity type impurity (N), thereby providing the first conductivity type well (P^{*}) having an impurity concentration lower than the remaining first conductivity type well or wells (P^{**}) formed in the semiconductor body. Alternately, the basic feature of this invention is that first conductivity type impurity is further doped into one or more of the first conductivity type low impurity concentration wells (P, P^{*}) to form at least one first conductivity type well of high impurity concentration (P^{**}). In this way, there can be obtained three different types of first conductivity type (P) regions, that is, the semiconductor body (P) itself, the first conductivity type well (P^{**}) formed in the semiconductor body, and the first conductivity type well (P^{*}) having the first conductivity type impurity concentration lowered by the doped second conductivity type impurity. Further, in a case where two different types of second conductivity type (N) wells are formed, or where two or more different types of first conductivity type (P) wells are formed, first conductivity type wells having more different degrees of impurity concentration can be obtained. If the structure is applied to the dynamic random access memory, it is preferable to form cells in one of the first conductivity type wells having the highest impurity concentration. This is because the leak current in the memory capacitor is required to be lowered and the soft error is required to be minimum.

Further, in this invention, it is possible to divide an ion-implantation step into a plurality of substeps and form a plurality of wells of variously selected degrees of impurity concentration by controlling the amount of impurity doped into each portion of the semiconductor substrate.

This invention can be more fully understood

from the following detailed description when taken in conjunction with the accompanying drawings, in which:

Fig. 1 is a cross sectional view of a semiconductor device with the conventional well structure;

Figs. 2A to 2C are cross sectional views showing the manufacturing process of a semiconductor device with well structure according to one embodiment of this invention;

Figs. 3A to 3M are cross sectional views showing the manufacturing process in a case where a trench type DRAM and the peripheral circuit thereof are formed on an N-type substrate with well structure according to one embodiment of this invention;

Fig. 4 is a cross sectional view showing the case in which the DRAM shown in Fig. 3M is formed in a P-type substrate;

Fig. 5 is a cross sectional view of a modification of the DRAM shown in Fig. 4;

Fig. 6 is a cross sectional view showing the case in which the DRAM shown in Fig. 5 is formed in a P-type substrate;

Fig. 7 is a cross sectional view of another modification of the DRAM shown in Fig. 4;

Fig. 8 is a cross sectional view of a modification of the DRAM which is shown in Fig. 3M and in which various power source voltages are applied;

Fig. 9A shows a voltage ganerating circuit for supplying low voltage VCC to the multi-power source DRAM shown in Fig. 8;

Fig. 9B shows a voltage generating circuit for supplying low voltage VBB to the multi-power source DRAM shown in Fig. 8;

Fig. 10 is a cross sectional view showing the structure of a trench cell type memory which can be applied to a DRAM utilizing this invention;

Fig. 11 is a cross sectional view showing the structure of a stacked cell type memory which can be applied to a DRAM utilizing this invention;

Fig. 12 is a cross sectional view showing the structure of a stacked trench (STT) cell type memory which can be applied to a DRAM utilizing this invention;

Fig. 13 is a cross sectional view showing the structure of a planar cell type memory which can be applied to a DRAM utilizing this invention;

Fig. 14 is a cross sectional view showing the structure of an SRAM which can be applied to this invention; and

Figs. 15A to 15E respectively show various CMOS inverters to which the present invention can be applied.

There will now be described an embodiment of this invention with reference to the drawings. First, as shown in Fig. 2A, boron is ion-implanted using the photolithographic method into that part of P-type semiconductor body 101 which is allocated for formation of first P-well region 102-1 of cell area A in a dynamic RAM. In this case, the ion-implantation dosage amount is 2×10^{14} cm^{-2} and the acceleration voltage is 100 keV. At the same time, boron is also ion-implanted into that part which is allocated for formation of second P-well region 102-2 of peripheral circuit section B. After this, the semiconductor structure is subjected to a first heat treatment at a temperature of 1190 °C in an N_2 gas atmosphere for about 6 hours so as to form P-well regions 102-1 and 102-2. Fig. 2A shows the semiconductor structure after the heat treatment. In Fig. 2A, xxx indicates ion-implanted boron.

Next, phosphorus 104 is ion-implanted into a portion which is allocated for formation of first N-well region 106 and internal portion 105 of second P-type well 102-2 by using resist film 103 with the dose amount of 5×10^{13} cm^{-2} and at an acceleration voltage of 100 keV. After this, the semiconductor structure is subjected to a second heat treatment at a temperature of 1190 °C in an N_2 gas atmosphere for about 4 hours. As a result, first P-well region (P^{++}) 107 having a surface impurity concentration of 5×10^{17} cm^{-3} is formed in cell area A, and second P-well region (P^{+}) 105 having a surface impurity concentration of 2×10^{17} cm^{-3} is formed in the N-channel region of peripheral circuit B.

Then, capacitor insulation film 108, storage electrode (polysilicon) 109, N^{+}-type diffusion layer 110, gate electrode (polysilicon) 111 of a write-in/readout transistor, and wiring layer (aluminum) 112 for the bit line are formed in cell area A. Further, gate electrode (polysilicon) 113 of an N-channel transistor, gate electrode (polysilicon) 114 of a P-channel transistor, diffusion regions 115 and 116, and lead-out wiring layer (aluminum) 117 for each electrode are formed in second P-well 105 and first N-well 106 of the peripheral circuit such as row/column decoders and sense amplifiers, thus forming a CMOS DRAM as shown in Fig. 2C.

Figs. 3A to 3M are cross sectional views showing the manufacturing process used in a case where a trench type DRAM cell and the peripheral circuit thereof are formed on an N-type substrate with a well structure according to one embodiment of this invention.

As shown in Fig. 3A, resist film 303A is formed (patterning) on a predetermined portion of N-type substrate 301 covered with SiO_2 oxide film 302A having a thickness of about 1000 Å, and boron (P-type impurity) is ion-implanted via the openings of resist film 303A with the dose amount of 2×10^{13} cm^{-2} and at an acceleration voltage of 100 keV. As the result of the ion-implantation process, P-type impurity region 304A is formed in that portion of N-type substrate 301 which lies under the openings of resist film 303A.

Then, as shown in Fig. 3B, new resist film 303B is formed to have openings, and boron is ion-implanted via the openings of resist film 303B with the dose amount of 3 × 10^{13} cm^{-2} and at an acceleration voltage of 100 keV. As the result of the ion-implantation process, P-type impurity region 304B and P-type impurity region (304A + 304B) are formed in N-type substrate 301 in addition to P-type impurity region 304A.

After this, resist film 303B is removed and the semiconductor structure is subjected to a heat treatment in the N_2 gas atmosphere at a temperature of 1190°C for 6 hours. As a result, P-type impurity regions 304A, 304B, and (304A + 304B) are thermally diffused (drive-in diffusion of P-well) to form P-well-2 having a low impurity concentration (P), P-well-3 having a mid range impurity concentration (P^+), and P-well-1 having a high impurity concentration (P^{++}), as shown in Fig. 3C.

Then, as shown in Fig. 3D, new resist film 303D is formed to have openings, and phosphorus (N-type impurity) is ion-implanted via the openings of resist film 303D with the dose amount of 3 × 10^{13} cm^{-2} and at an acceleration voltage of 160 keV. As the result of the ion-implantation process, N-type impurity regions 306D are formed in N-type substrate 301 and P-well-2.

After this, resist film 303D is removed and the semiconductor structure is subjected to a heat treatment in the N_2 gas atmosphere at a temperature of 1190°C for 4 hours. As a result, N-type impurity regions 306D are thermally diffused (drive-in diffusion of N-well) to form N-well-1 and N-well-2 in N-type substrate 301 and P-well-2, respectively, as shown in Fig. 3E.

In the thermal diffusion process, N-type impurity of N-well-2 is partly neutralized by P-type impurity of P-well-2, thus setting the impurity concentration (N) of N-well-2 lower than that (N^+) of N-well-1.

Then, oxide film 302A is removed and field oxide film 302F is formed as shown in Fig. 3F. After this, thick resist film 302G is formed on the semiconductor structure, and trench 310 for the memory cell capacitor is formed in a predetermined portion of P-well-1 by means of a reactive ion etching (RIE) method, or by use of a laser beam as shown in Fig. 3G. Thereafter, a thermal oxide film (SiO_2) having a thickness of about 200 Å is formed on the silicon substrate, where from the resist was removed.

Next trench 310 and its peripheral thermal oxide film (SiO_2) are etched, a portion of field oxide film 302G around trench 310 is selectively removed, and a doped polysilicon layer (not shown) having an N-type impurity to be diffused into the surface area of trench 310 is formed on the semiconductor structure. Then, the semiconductor structure is subjected to a heat treatment to diffuse the N-type impurity from the doped polysilicon layer formed thereon into the surface area of trench 310, thus forming diffusion layer 311 of the capacitor electrode, as shown in Fig. 3H. The doped polysilicon layer is then removed after diffusion layer 311 has been formed.

As shown in Fig. 3I, after heat oxide film 302H has been removed, extremely thin SiO_2 film 302I of 100 Å is formed on surface substrate 301 which has diffusion layer 311 formed therein. Oxide film 302I is used as dielectric material of the memory capacitor. Polysilicon layer 312 of the capacitor electrode is formed around and on the internal surface of trench 310, with part of dielectric oxide film 302I disposed between polysilicon layer 312 and diffusion layer 311.

After this, the substrate surface is subjected to an oxidation process whereby oxide film 302J having a predetermined thickness (for example, 200 Å) is formed on substrate 301, and then polysilicon layer 313 to be used as a gate electrode is formed on oxide film 302J as shown in Fig. 3J.

Next, N-type diffusion regions 308 which form source and drain regions are formed on both sides of respective electrodes 313 of P-well-1 and P-well-3 by use of a resist film (not shown) as shown in Fig. 3K. Further, N-type diffusion layers 308 are formed in the end portions of N-well-1 and N-well-2.

Then, as shown in Fig. 3L, P-type diffusion layers 309 are formed in the end portions of P-well-1 to P-well-3 by use of a resist film (not shown). Further, P-type diffusion regions 309 which form source and drain regions are formed on both sides of respective electrodes 313 of N-well-1 and N-well-2.

Next, as shown in Fig. 3M, thick SiO_2 film 302M is formed on the entire surface of substrate 301, predetermined portions of second oxide film 302M are etched out to form openings, and aluminum wiring layers 314 are selectively formed in connection with respective N-type diffusion layers 308, P-type diffusion layers 309, and capacitor electrode 312, via the openings.

In Fig. 3M, P-channel transistors, constituting a power source voltage converting circuit, input/output circuit, input protection circuit, and the like, are formed in N-well-1, and P-channel transistors, constituting a sense amplifier and the like, are formed in N-well-2. Further, memory cells, and N-channel transistors, constituting sense amplifier, word driver, and the like, are formed in that one of P-well-1 to P-well-3 which has the highest impurity concentration, that is, P-well-1. In addition, the peripheral circuit and the like are formed in P-well-2.

Since N-well-2 is isolated from N-well-1 by means of P-well-2, voltages applied to N-well-1 and

N-well-2 can be set to have different voltage levels. Further, it is possible that an N-well having an impurity concentration higher than that of P-well-1 (P^{++}) be provided in a position which is not shown in the drawing.

Fig. 4 shows the case in which the DRAM shown in Fig. 3M is formed in a P-type substrate. N-well-2 is formed in P-well-2 in Fig. 3M, but P-well-2 is formed in N-well-3 in Fig. 4.

Fig. 5 is a modification of the DRAM shown in Fig. 4. In Fig. 5, P-well-1 of the memory cell is formed in N-well-2, and N-well-1' in P-well-2 is formed in the same step as that of N-well-1, or it is formed immediately after the step of forming N-well-1.

Fig. 6 shows the case wherein the DRAM shown in Fig. 5 is formed in a P-type substrate. The structure shown in Fig. 6 is similar to that of Fig. 5 except that the impurity conductivity type is inverted from either a P-type impurity to N-type impurity or vice versa.

Fig. 7 is another modification of the DRAM shown in Fig. 4. In this embodiment, N-well-1 has the highest impurity concentration (N^{++}), and a memory cell is formed therein. The peripheral circuit of the DRAM is formed in N-well-2 which has a lower impurity concentration than N-well-1. The term "highest impurity concentration" used in this embodiment refers to N-type impurity, and therefore P-well-1 may be formed to have a P-type impurity concentration which is higher than an N-type impurity concentration of N-well-1, for example.

Fig. 8 is a modification of the DRAM shown in Fig. 3M to which various power source voltages are applied. In this embodiment, external power source voltage ExtVCC (+5 V) is applied to N-well-1 wherein P-channel transistors constituting the input/output circuit and the like are formed. Internal power source voltage IntVCC (+4 V) which is derived by means of such a voltage generating circuit as shown in Fig. 9A is applied to N-well-1 formed in P-well-2. With the structure shown in Fig. 8, the pn junction between N-well-1 and P-well-2 is reversely biased because of the potential difference between ExtVCC (+5 V) and IntVCC (+4 V) so that N-well-1 is electrically isolated from P-well-2. Therefore, ExtVCC (+5 V) can be applied to the input/output circuit which requires a relatively high operation voltage, while at the same time IntVCC (+4 V or less) can be applied to the internal circuit which is desirably operated at a low voltage level.

Further, low negative voltage IntVBB (-2 V) which is applied to the memory cell in P-well-1, for example, can be derived from such a voltage generating circuit as shown in Fig. 9B.

Because the junction between P-well-1 and the N-type substrate is reversely biased by the potential difference between EXtVCC (+5 V) or IntVCC (+4 V) and IntVBB (-2 V), the low negative voltage IntVBB (-2 V) can thus be used. In other words, since bias voltages of various levels can be applied to the respective wells, the drain-source voltage of the transistor formed in the well can be freely set.

Incidentally, CMOS inverters shown in Figs. 15A to 15E can be applied to the device of this invention.

The circuits shown in Figs. 9A and 9B are disclosed in the following documents:
1986 IEEE International Solid-State Circuits Conference ISSCC 86 / FRIDAY, FEBRUARY 21, 1986 SESSION XIX: DYNAMIC RAMs pages 272-273
FAM 19.7: An Experimental 4Mb CMOS DRAM
Tohru Furuyama, Takashi Ohsawa, Yoji Watanabe, Hidemi Ishiuchi, Takeshi Tanaka, Kazunori Ohuchi, Hiroyuki Tango, Kenji Natori, Osamu Ozawa
Toshiba Semiconductor Device Engineering Laboratory/VLSI Research Center Kawasaki, Japan

Fig. 10 shows the structure of a trench cell type memory which can be applied to a DRAM utilizing this invention. This structure is the same as that of Fig. 3M (however, the conductivity type of substrate 301 can be P or N). Gate electrode 313 is used as a word line of the memory cell, and the aluminum wiring layer connected to diffusion region 308 which lies on the left side in Fig. 10 is used as a bit line of the memory cell.

Examples of trench type memories having structures other than those mentioned above are disclosed in the following U.S. Patent specifications:

United States Patent Patent Number: 4,672,410
Miura et al. January 9, 1987
"SEMICONDUCTOR MEMORY DEVICE WITH TRENCH SURROUNDING EACH MEMORY CELL"
United States Patent Patent Number: 4,673,962
Chatterjee et al. January 16, 1987
"VERTICAL DRAM CELL AND METHOD"
It should be understood that the contents disclosed in the above U.S. Patent specifications are incorporated in this application.

Fig. 11 shows the structure of a stacked cell type memory which can be applied to a DRAM utilizing this invention. In the stacked cell type memory, a memory capacitor is constituted by concave pot type polysilicon storage node 312B and convex capacitor electrode 312A which is engaged with a concave portion of storage node 312B, via an oxide film (dielectric material), with a thickness of several tens Å.

Fig. 12 shows the structure of a stacked trench (STT) cell type memory which can be applied to a DRAM utilizing this invention. The STT structure can be attained by applying the stacked cell structure of Fig. 11 to the trench structure of Fig. 10. The STT structure used in this invention is suitable

for DRAM of a large memory capacity, for example, 16 M bits.

Fig. 13 shows the structure of a planar cell type memory which can be applied to a DRAM utilizing this invention. This structure corresponds to the cell structure in area A of Fig. 2C.

Fig. 14 shows the structure of an SRAM which can be applied to this invention. In this embodiment, the drain wiring layer of the cell transistor is formed in the form of two-layered structure having first polysilicon layer (for internal wiring layer) 312F of low resistance and second polysilicon layer (for load resistor) 312G of high resistance.

The Bipolar-CMOS technology disclosed in the following documents can be applied as the conventional memory cell technology which can be used in this invention:

IEEE JOURNAL OF SOLID-STATE CIRCUITS, VOL. SC-22, No. 5, OCTOBER 1987
"An Experimental 1-Mbit BiCMOS DRAM" pages 657-662
GORO KITSUKAWA, RYOICHI HORI, YOSHIKI KAWAJIRI, TAKAO WATANABE, TAKAYUKI KAWAHARA, KIYOO ITOH, YUTAKA KOBAYASHI, MASAYUKI OOHAYASHI, KYOICHIRO ASAYAMA, TAKAHIDE IKEDA, AND HIROSHI KAWAMOTO
408-IEDM86
"Advanced BiCMOS Technology for High Speed VLSI" pages 408-411
T. Ikeda *, T. Nagano, N. Momma, K. Miyata, H. Higuchi **, M. Odaka *, K. Ogiue *.
Hitachi Research Laboratory, 4029, Kuji-cho, Hitachi-shi, Ibaraki, 319-12, Japan
802-IEDM86
"Bipolar CMOS merged structure for high speed M bit DRAM" pages 802-804
Y. Kobayashi, M. Oohayashi, K. Asayama, T. Ikeda * R. Hori ** and K. Itoh **
Hitachi Research Laboratory, Hitachi, Ltd., Hitachi, Ibaraki, Japan, 319-12

Bipolar devices, which appear to be similar to but are substantially different from the semiconductor device of this invention, are disclosed in the following documents:

Physics and Technology of Semiconductor Devices page 209
A.S. GROVE
Fairchild Semiconductor, Palo Alto University of California, Berkeley
John Wiley and Sons, Inc., New York * London * Sydney
Physics of Semiconductor Devices
SECOND EDITION pages 192-197
S.M. Sze.
Bell. Laboratories, Incorporated Murray Hill, New Jersey
A WILEY-INTERSCIENCE PUBLICATION JOHN WILEY & SONS
New York * Chichester * Brisbane * Toronto * Singapore

In general, the bipolar device includes high impurity concentration regions and low impurity concentration regions, but they are substantially different from the well of high impurity concentration (P^{++}) and the wells of lower impurity concentration (P^{+}, P) of this invention. More specifically, an active circuit element such as a memory cell is formed in the high impurity concentration (P^{++}) well in this invention, but in the bipolar device, the high impurity concentration region (for example, emitter) is used as part of the active circuit element. It should be understood that the structure of this invention (combination of the high and low impurity concentration wells) is essentially different from that of the bipolar device (combination of low and high impurity concentration regions such as the emitter and collector).

This invention is not limited to the embodiments described above, and can be variously modified. For example, in the embodiment of Fig. 2C, a P-well of low impurity concentration is formed in peripheral circuit section B by using opposite conductivity type (P-type against N-type, for example) impurity. However, it is possible to form a P-well of high impurity concentration in cell section A by using the same conductivity type (P-type for P-type, for example) impurity to enhance the impurity concentration of the well. Further, in the embodiment, first N-well is formed in the first P-well to form the second P-well with impurity concentration lower than that of the first P-well. However, it is also possible to form low and high impurity concentration N-wells by forming a first N-well with impurity concentration higher than that of

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** Central Research Laboratory, Hitachi, Ltd., Kokubunji, Tokyo, Japan 185

the first P-well in the first P-well.

As described above, according to this invention, wells with various degrees of impurity concentration can be easily formed, and therefore the wells can be selectively used to attain desired elements. In the DRAM or the like, a cell or cells can be formed in the well of the highest impurity concentration and the peripheral circuit section can be formed in the well with the impurity concentration next to the highest impurity concentration, thus making it possible to significantly improve the performance and characteristics of the semiconductor device.

Claims

1. A semiconductor device comprising:

a semiconductor substrate (301);

a first well (P-well-1) of a first conductivity type (P) formed in said semiconductor substrate (301);

a second well (P-well-2) of the first conductivity type (P) formed separately from said first well (P-well-1) in said semiconductor substrate (301), the surface impurity concentration (P) of said second well (P-well-2) being set lower than that (P^{++}) of said first well (P-well-1);

a memory cell structure formed in said first well (P-well-1); and

a transistor structure formed in said second well (P-well-2) to function in combination with said memory cell structure.

2. A semiconductor device according to claim 1, characterized by further comprising:

a third well (N-well-2) of a second conductivity type (N) formed separately from said semiconductor substrate (301) in said second well (P-well-2), a PN junction between said third well (N-well-2) and said second well (P-well-2) or between said second well (P-well-2) and said semiconductor substrate (301) being reversely biased by a potential difference between the potential of said semiconductor substrate (301) and that of said third well (N-well-2) to thereby electrically isolate said third well (N-well-2) from the other wells, wherein at least part of said transistor structure is formed in said third well (N-well-2).

3. A semiconductor device according to claim 2, characterized by further comprising:

a fourth well (P-well-3) of the first conductivity type (P) formed separately from said first well (P-well-1) and said second well (P-well-2) in said semiconductor substrate (301), said fourth well (P-well-3) having an impurity concentration (P^{+}) set lower than that (P^{++}) of said first well (P-well-1) and having a second transistor structure formed therein to be used in combination with said memory cell structure.

4. A semiconductor device according to claim 3, characterized by further comprising:

a fifth well (N-well-1) of the second conductivity type (N) formed separately from said first well (P-well-1), said second well (P-well-2), said fourth well (P-well-3), and said semiconductor substrate (301), a third transistor structure to be used in combination with said memory cell structure being formed in said fifth well (N-well-1).

5. A semiconductor device according to claim 3, characterized in that the impurity concentration (P^{+}) of said fourth well (P-well-3) is set lower than that (P^{++}) of said first well (P-well-1) and higher than that (P) of said second well (P-well-2).

6. A semiconductor device according to any one of claims 1 to 5, characterized in that an impurity of the second conductivity type (N) is injected and diffused into a high impurity concentration (P^{++}) region of the first conductivity type (P) region.

7. A semiconductor device according to claim 4, characterized in that the impurity concentration (N^{+}) of said third well (N-well-2) is set lower than that (N) of said fifth well (N-well-1).

8. A semiconductor device according to any one of claims 2 to 5, characterized by further comprising:

voltage supplying means (Fig. 9A) for supplying a potential (+4 V) different from that (+5 V) of said semiconductor substrate (301) to said third well (N-well-1, N-well-2), characterized in that said semiconductor substrate (301) is of the second conductivity type (N).

9. A semiconductor device according to claim 8, characterized in that at least one well of the second conductivity type (N) (N-well-1, N-well-2) is formed in said second well (P-well-2), and each of said second conductivity type wells is supplied with an independent potential.

10. A semiconductor device according to claim 8, characterized in that the potential (+5 V) of said semiconductor substrate (301) is applied from an external power source (ExtVCC) of the semiconductor device, and said voltage supplying means (Fig. 9A) includes a voltage converting circuit for converting the output potential of said external source (ExtVCC) to a different potential (+4 V).

11. A semiconductor device according to claim 10, characterized in that said voltage converting circuit (Fig. 9A) is formed in a well (N-well-1) formed separately from said first well (P-well-1) and said second well (P-well-2) in said semiconductor substrate (301).

12. A semiconductor device according to any one of claims 1 to 5, characterized in that said first well (P-well-1) is formed in a well (N-well-2) of the

second conductivity type (N) which is formed separately from the other wells in said semiconductor substrate (301).

13. A semiconductor device according to any one of claims 1 to 5, characterized in that said memory cell has a DRAM structure (Figs. 10 to 13) and includes a memory cell capacitor section (311-312) and an MOS transistor section (308, 313) for charging and discharging said memory cell capacitor section (311, 312).

14. A semiconductor device according to claim 13, characterized in that said memory cell capacitor section (311, 312) has a trench cell structure (Fig. 10).

15. A semiconductor device according to claim 13, characterized in that said memory cell capacitor section (311, 312) has a stacked cell structure (Fig. 11).

16. A semiconductor device according to claim 13, characterized in that said memory cell capacitor section (311, 312) has a stacked trench cell structure (Fig. 12).

17. A semiconductor device according to claim 13, characterized in that said memory cell capacitor section (311, 312) has a planar cell structure (Fig. 13).

18. A semiconductor device according to any one of claims 1 to 5, characterized in that said memory cell structure has a SRAM structure (Fig. 14).

19. A semiconductor device according to claim 1, characterized in that the impurity concentration of said second well (P-well-2, 102-2), which is lower than that of said first well (P-well-2, 102-1), is obtained by doping and diffusing an impurity of the second conductivity type (N) into said second well (P-well-2) having a first conductivity type (P).

20. A semiconductor device according to claim 3 or 19, characterized in that the impurity concentration of said fourth well (P-well-3), which is lower than that of said first well (P-well-1), is obtained by doping and diffusing an impurity of the second conductivity type (N) into said fourth well (P-well-3) having a first conductivity type (P).

21. A semiconductor device according to claim 1, characterized in that the impurity concentration of said first well (P-well-1, 102-1), which is higher than that of said second well (P-well-2, 102-2), is obtained by doping and diffusing an impurity of the first conductivity type (P) into said first well (P-well-1) having a first conductivity type (P).

22. A semiconductor device according to claim 3 or 21, characterized in that the impurity concentration of said first well (P-well-1, 102-1), which is higher than that of said fourth well (P-well-3), is obtained by doping and diffusing an impurity of the first conductivity type (P) into said first well (P-well-1) having a first conductivity type (P).

23. A semiconductor device comprising:

a semiconductor substrate (101, 301);

a memory cell well (P^{**}, P-well-1) of a first conductivity type (P) formed in said semiconductor substrate (101, 301);

at least one peripheral circuit well (P^{*}, P-well-3) of the first conductivity type (P) formed separately from said memory cell well (P^{**} P-well-1) in said semiconductor substrate (101, 301), the surface impurity concentration (P^{*}) of said peripheral circuit well (P^{*}, P-well-3) being set lower than that (P^{**}) of said memory cell well (P^{**}, P-well-1);

a RAM memory cell structure formed in said memory cell well (P^{**}; P-well-1); and

a MOS transistor structure formed in said peripheral circuit well (P^{*}, P-well-3) to function in combination with said RAM memory cell structure.

24. A semiconductor device according to claim 23, characterized in that an impurity of the second conductivity type (N) is doped and diffused into said high impurity concentration (P^{**}) having a first conductivity type (P).

25. A semiconductor device comprising:

a semiconductor substrate (301 Fig. 3M) of one conductivity type (N);

a memory cell well (P-well-1) of the other conductivity type (P) formed in said semiconductor substrate (301);

a DRAM memory cell structure formed in said memory cell well (P^{**}, P-well-1);

a first peripheral circuit well (P-well-2) of the other conductivity type (P) formed separately from said memory cell well (P-well-1) in said semiconductor substrate (301), the impurity concentration (P^{*}) of said first peripheral circuit well (P-well-2) being set lower than that (P^{**}) of said memory cell well (P-well-1);

an internal well (N-well-2) of said one conductivity type (N) formed in said first peripheral circuit well (P-well-2) to include a first MOS transistor structure to be used in combination with said memory cell structure;

a second peripheral circuit well (P-well-3) formed separately from said memory cell well (P-well-1) in said semiconductor substrate (301) to include a second MOS transistor structure to be used in combination with said memory cell structure, the impurity concentration (P^{*}) of said second peripheral circuit well (P-well-3) being set lower than that (P^{**}) of said memory cell well (P-well-1); and

a third peripheral circuit well (N-well-1) formed separately from said memory cell well (P-well-1) in said semiconductor substrate (301) to include a third MOS transistor structure to be used in combination with said memory cell structure.

26. A semiconductor device comprising:

a semiconductor substrate (301/Fig. 6) of one conductivity type (N);

a first memory cell well (P-well-2) of the other conductivity type (P) formed in said semiconductor substrate (301);

a second memory cell well (N-well-1) of said one conductivity type (N) formed in said first memory cell well (P-well-2);

a DRAM memory cell structure formed in said second memory cell well (N-well-1);

a first peripheral circuit well (N-well-2) of said one conductivity type (N) formed separately from said first memory cell well (P-well-2) in said semiconductor substrate (301), the impurity concentration (N) of said first peripheral circuit well (N-well-2) being set lower than that (P^{++}) of said second memory cell well (N-well-1);

an internal well (P-well-1) of said other conductivity type (P) formed in said first peripheral circuit well (N-well-2) to include a first MOS transistor structure to be used in combination with said memory cell structure;

a second peripheral circuit well (N-well-3) formed separately from said first memory cell well (P-well-2) in said semiconductor substrate (301) to include a second MOS transistor structure to be used in combination with said memory cell structure, the impurity concentration (N^{+}) of said second peripheral circuit well (N-well-3) being set lower than that (N^{++}) of said second memory cell well (N-well-1); and

a third peripheral circuit well (P-well-1) formed separately from said first memory cell well (P-well-2) in said semiconductor substrate (301) to include a third MOS transistor structure to be used in combination with said memory cell structure.

27. A semiconductor device comprising:

a semiconductor substrate (301/Fig. 3M) of one conductivity type (N);

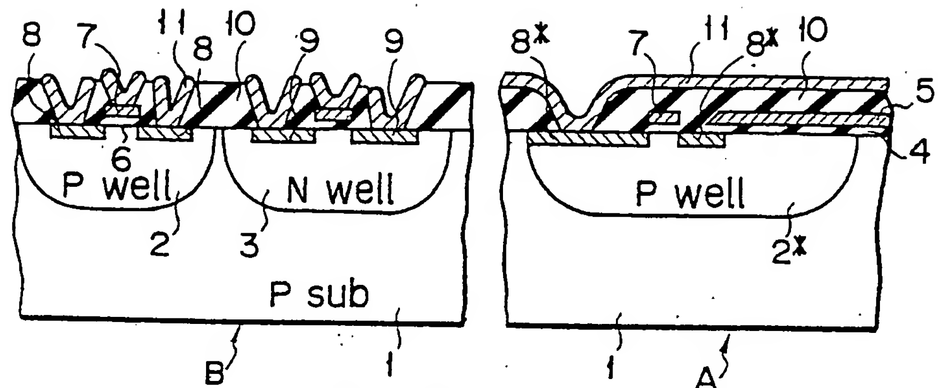
a memory cell well (P-well-1) of the other conductivity type (P) formed in said semiconductor substrate (301);

a DRAM memory cell structure formed in said memory cell well (P^{++}, P-well-1);

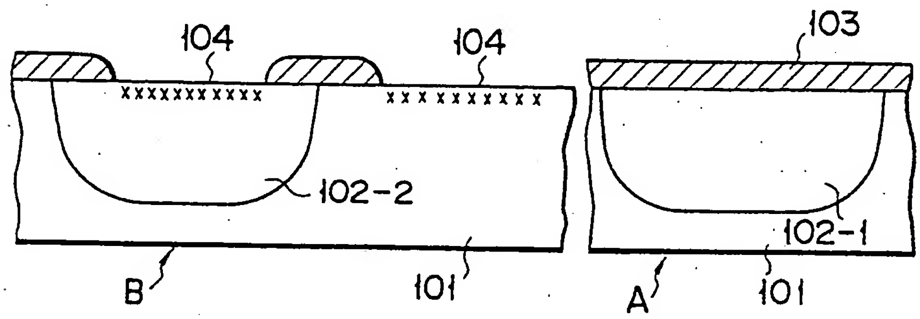
a first peripheral circuit well (P-well-2) of the other conductivity type (P) formed separately from said memory cell well (P-well-1) in said semiconductor substrate (301), the impurity concentration (P^{+}) of said first peripheral circuit well (P-well-2), being set lower than that (P^{++}) of said memory cell well (P-well-1);

an internal well (N-well-2) of said one conductivity type (N) formed in said first peripheral circuit well (P-well-2) to include a first MOS transistor structure to be used in combination with said memory cell structure; and

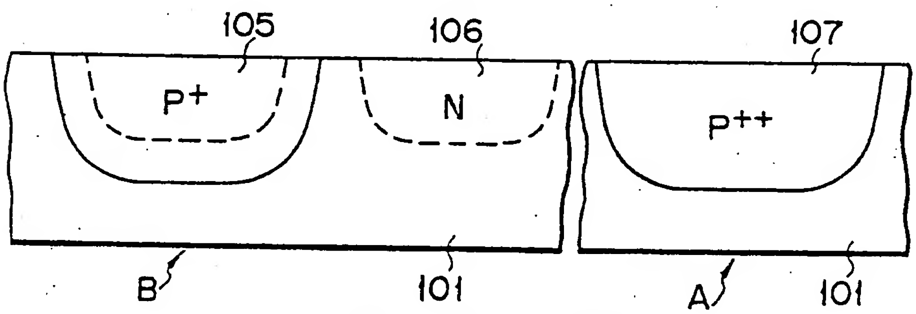
a second peripheral circuit well (N-well-1) formed separately from said memory cell well (P-well-1) in said semiconductor substrate (301) to include a second MOS transistor structure to be used in combination with said memory cell structure, the impurity concentration of said second peripheral circuit well (N-well-1) being set higher than that of said internal well (N-well-2) formed in said first peripheral circuit well (P-well-2).



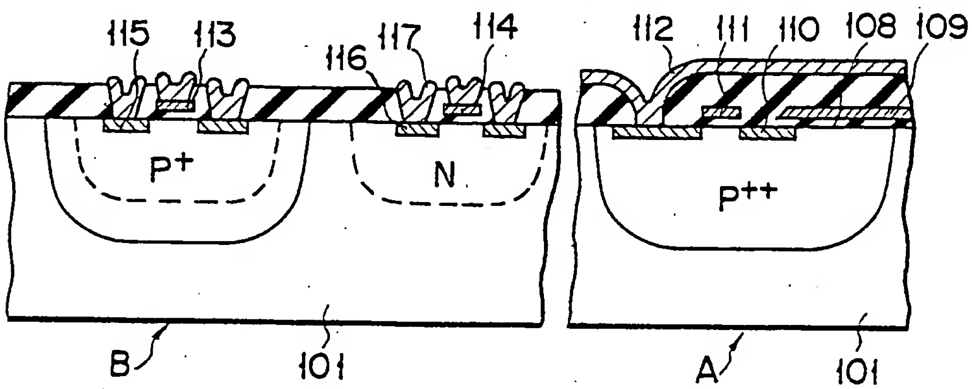
F I G. 1



F I G. 2A



F I G. 2B



F I G. 2C

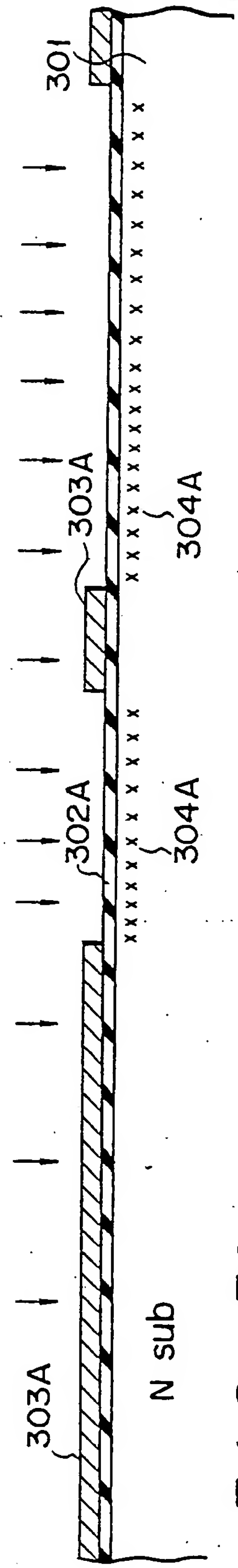


FIG. 3A

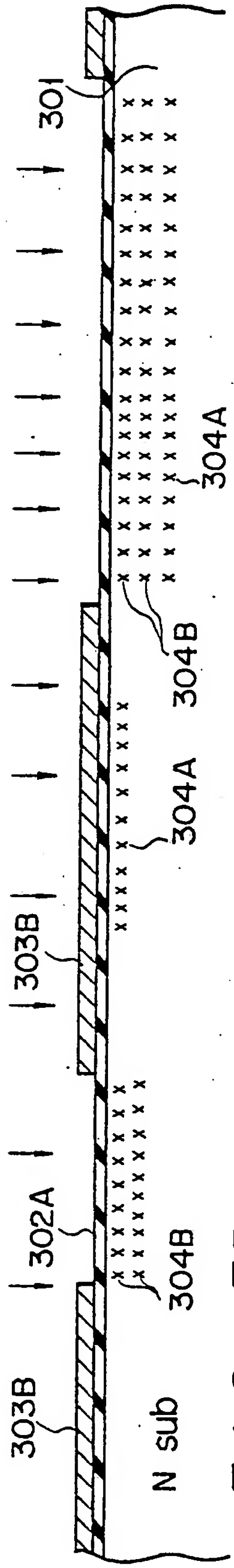


FIG. 3B

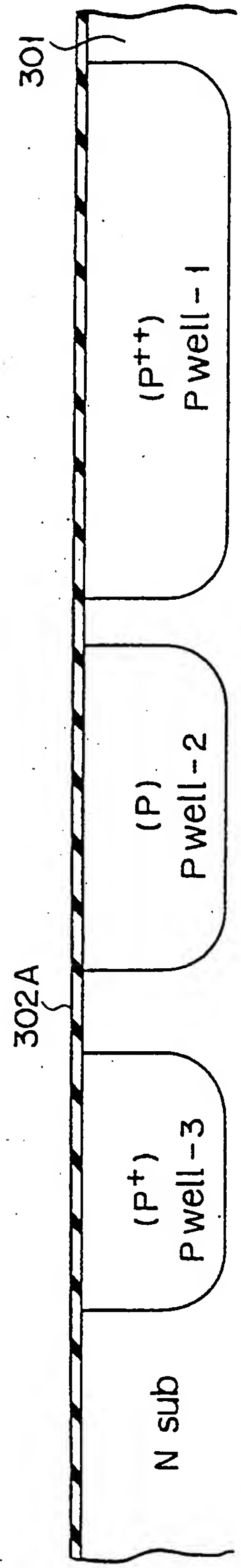
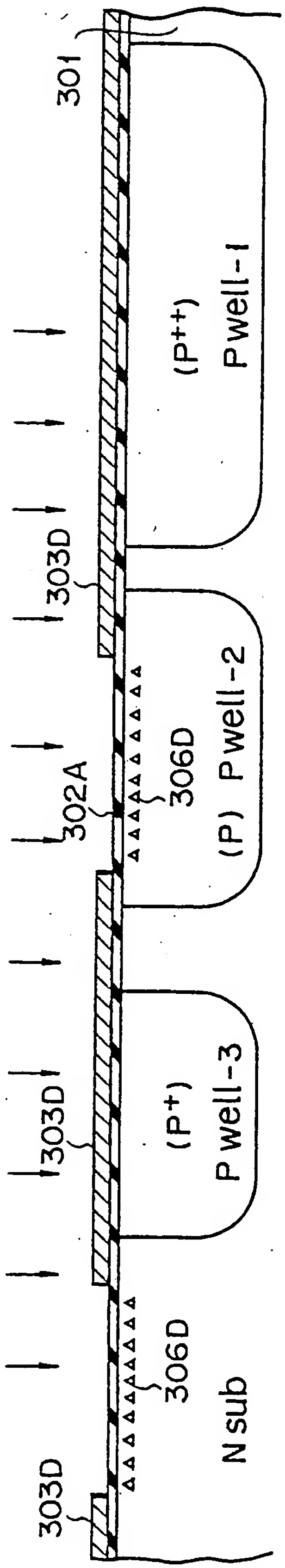
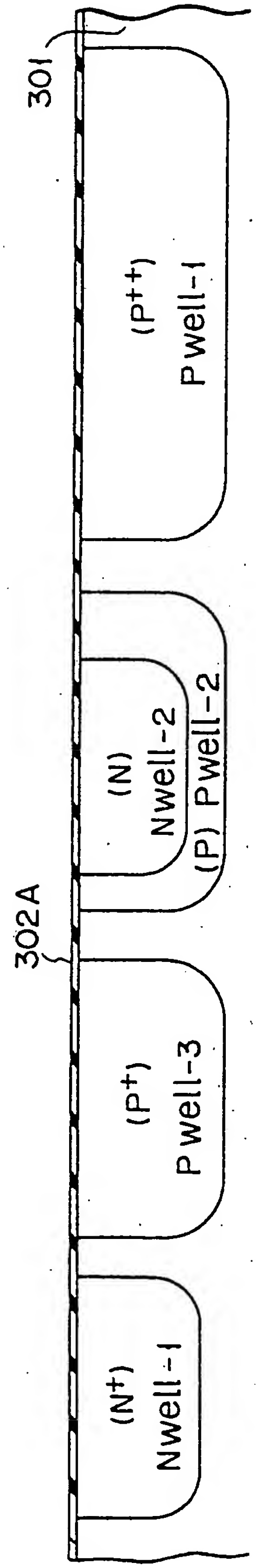


FIG. 3C


301
303D
302A
306D
303D
306D
303D
(P++)
P well-1
(P) P well-2
(P+)
P well-3
N sub

F I G. 3D


301
302A
(P++)
P well-1
(N)
Nwell-2
(P) Pwell-2
(P+)
P well-3
(N+)
Nwell-1

F I G. 3E

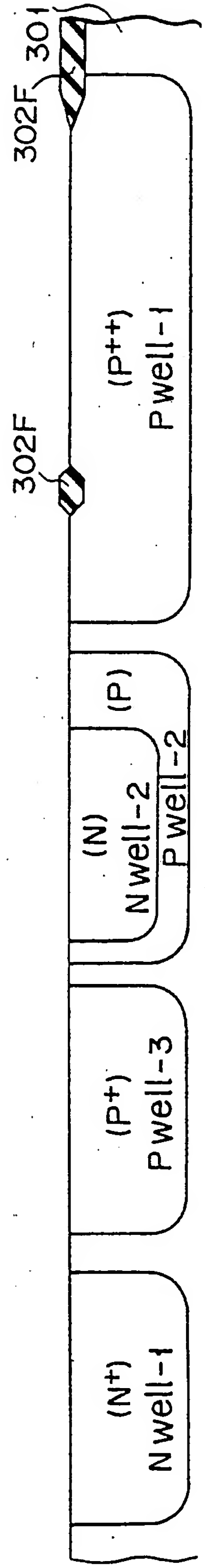


FIG. 3F

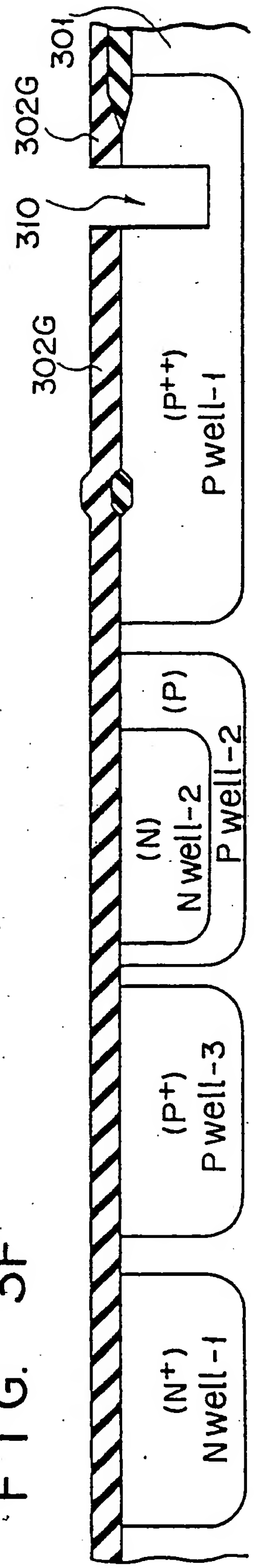


FIG. 3G

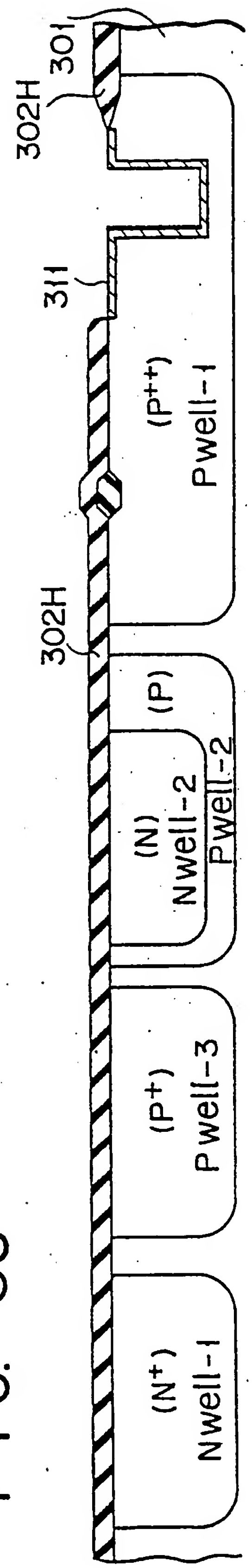


FIG. 3H

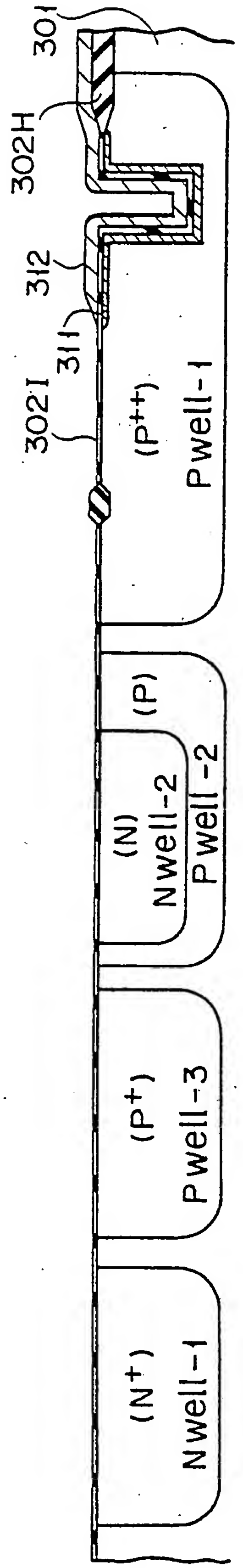


FIG. 3I

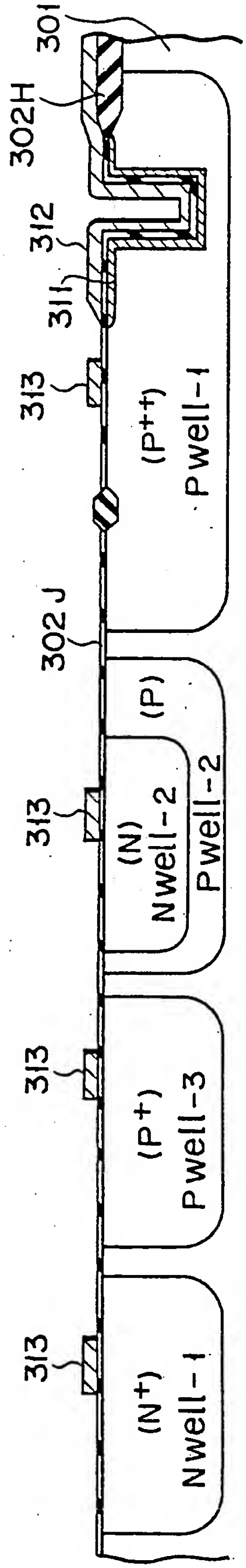


FIG. 3J

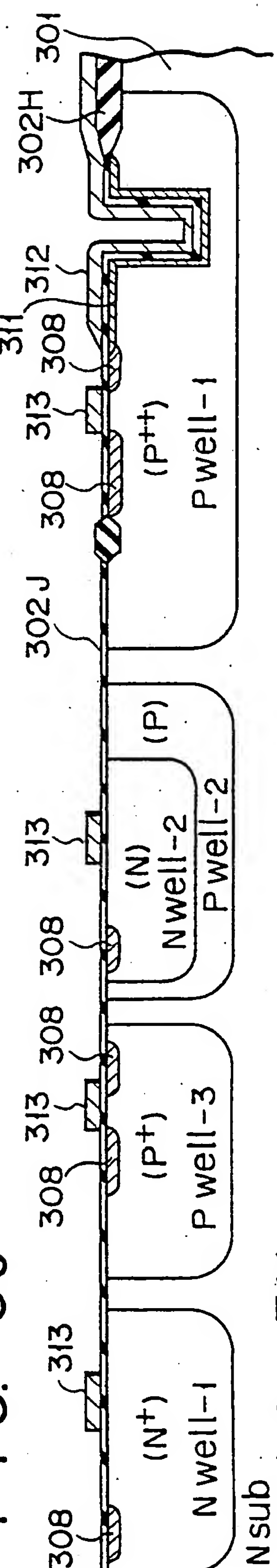


FIG. 3K

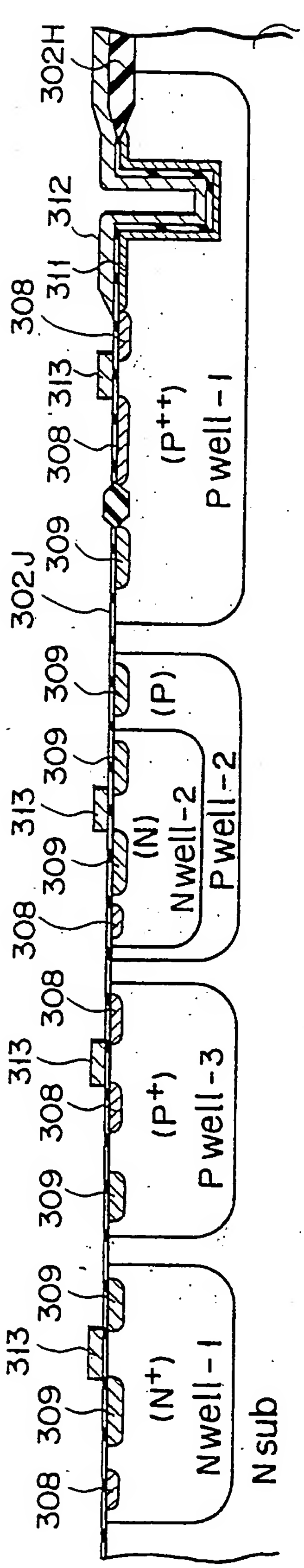

302H
301
312
311
308
313
309
302J
(P++)
P well-1
(P)
(N)
N well-2
P well-2
(P+)
P well-3
(N+)
N well-1
N sub

FIG. 3L

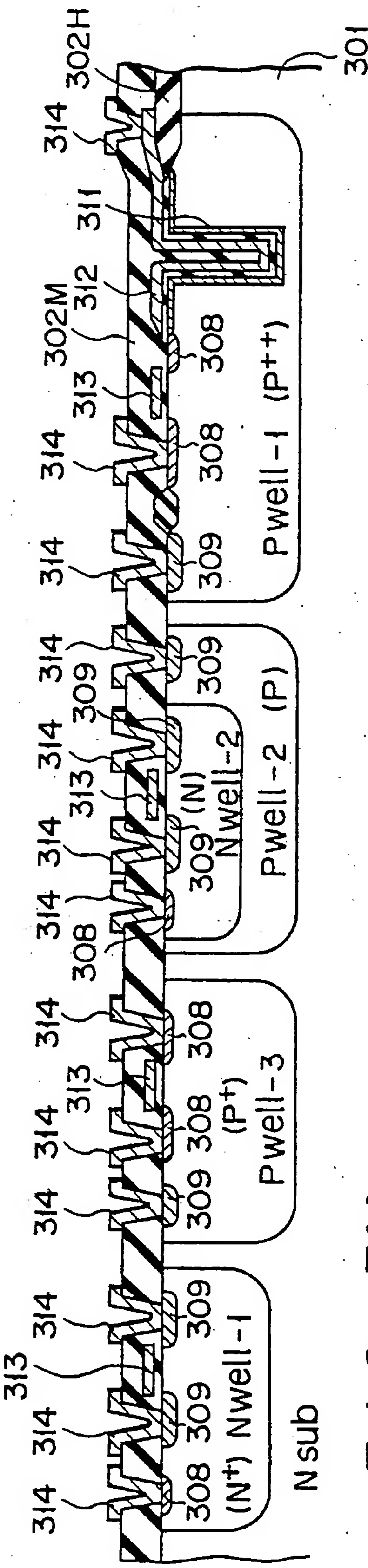

302H
301
314
311
312
302M
313
308
309
P well-1 (P++)
P well-2 (P)
(N)
N well-2
(P+)
P well-3
(N+) N well-1
N sub

FIG. 3M

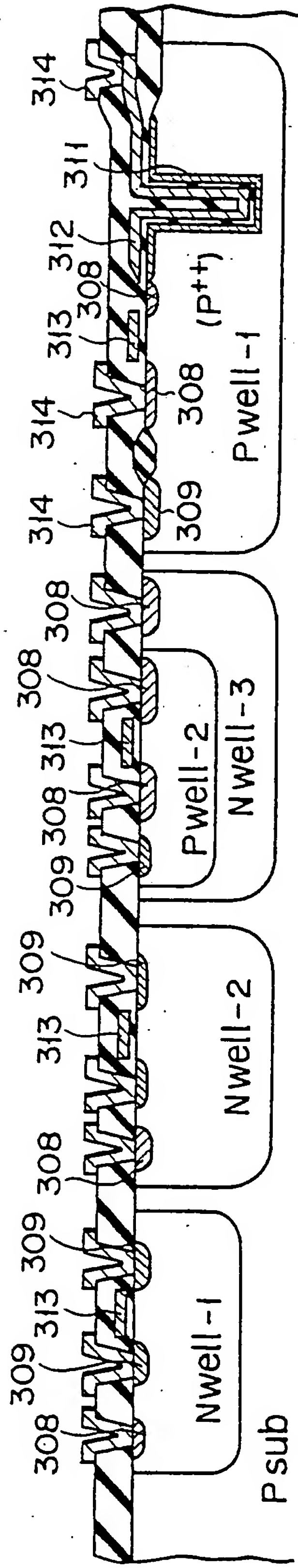


FIG. 4

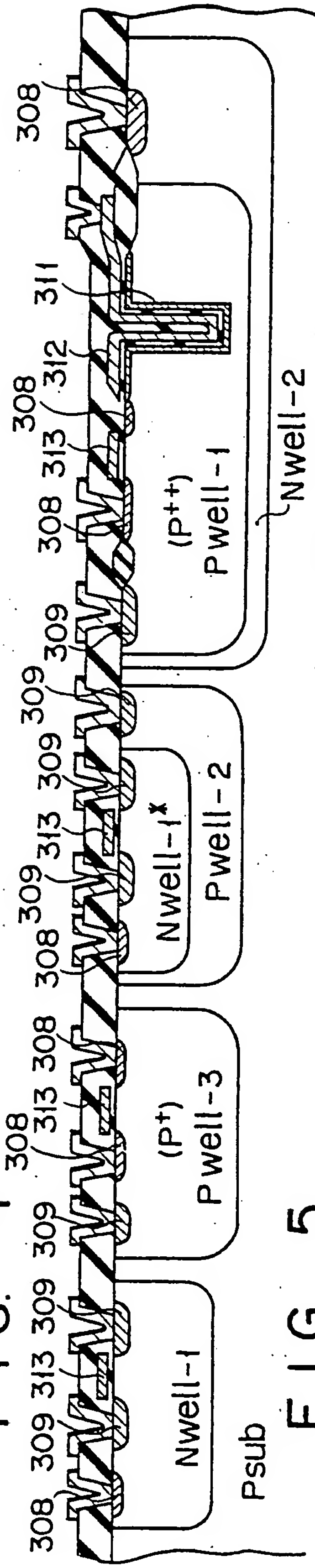


FIG. 5

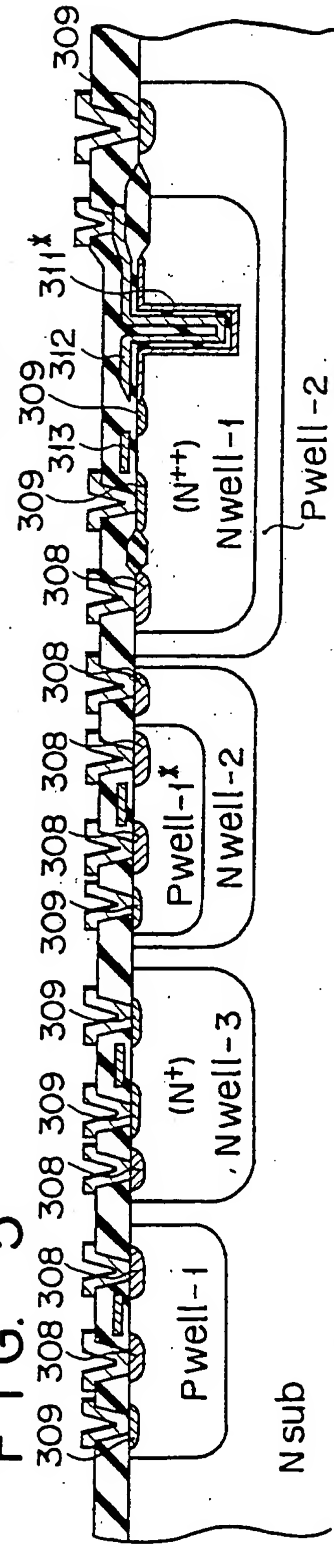


FIG. 6

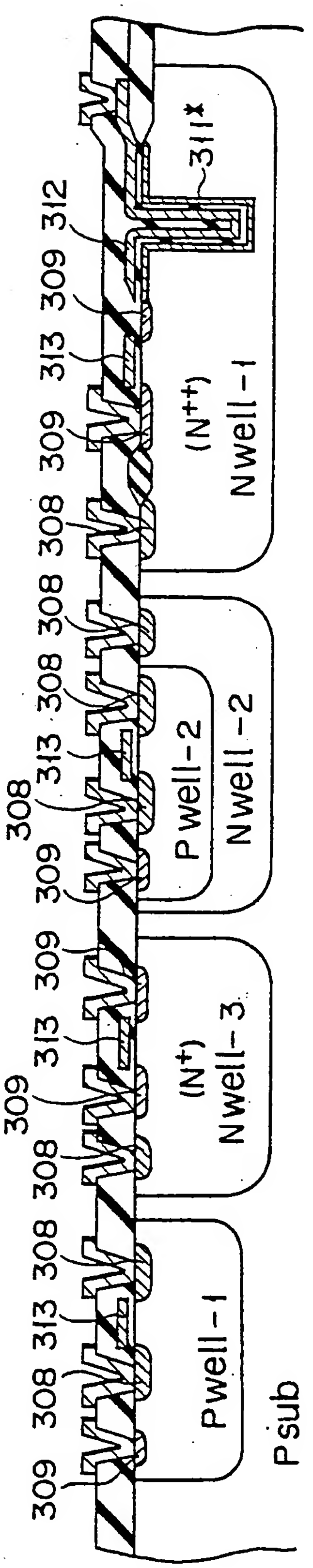

309
308
313
308
308
309
313
309
309
308
313
308
308
308
309
313
309
312
311*
Pwell-1
Psub
(N+)
Nwell-3
Pwell-2
Nwell-2
(N++)
Nwell-1

FIG. 7

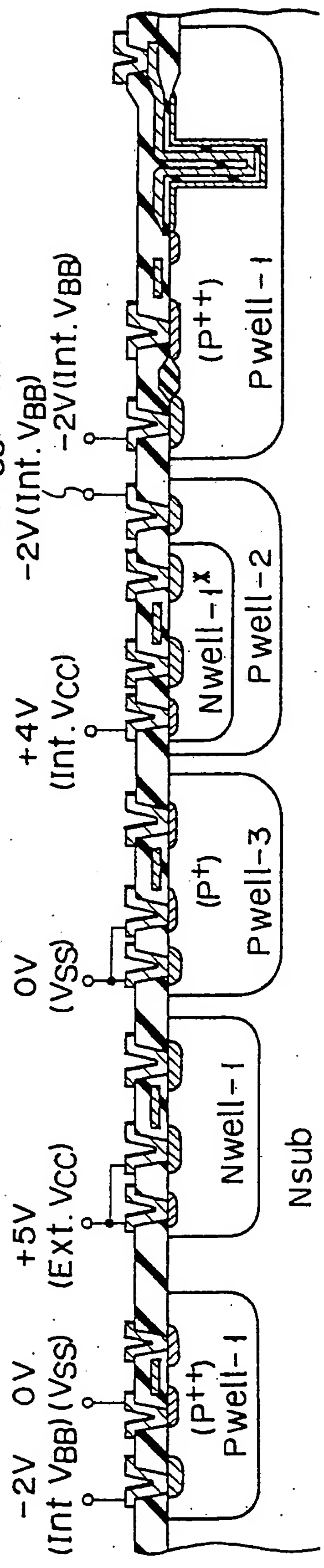
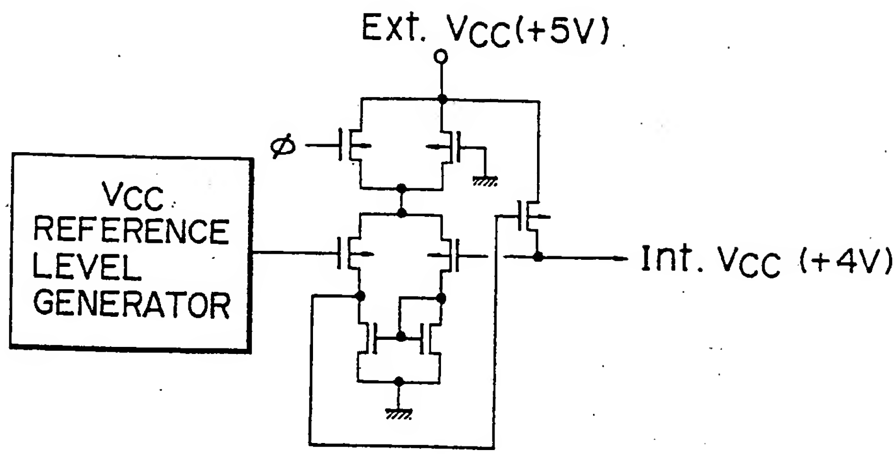
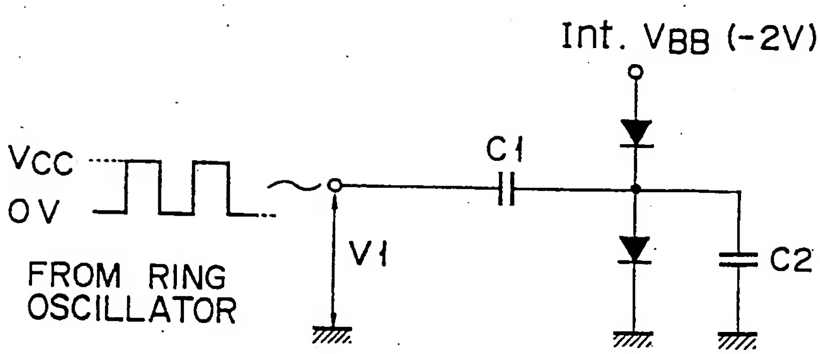

-2V
(Int VBB)
0V
(VSS)
+5V
(Ext. VCC)
0V
(VSS)
+4V
(Int. VCC)
0V(VSS) OR
-2V(Int. VBB)
-2V(Int. VBB)
(P++)
Pwell-1
Nwell-1
Nsub
(P+)
Pwell-3
Nwell-1*
Pwell-2
(P++)
Pwell-1

FIG. 8


Ext. VCC(+5V)
Ø
VCC REFERENCE LEVEL GENERATOR
Int. VCC (+4V)

F I G. 9A


Int. VBB (-2V)
VCC
0 V
FROM RING OSCILLATOR
C1
V1
C2

F I G. 9B

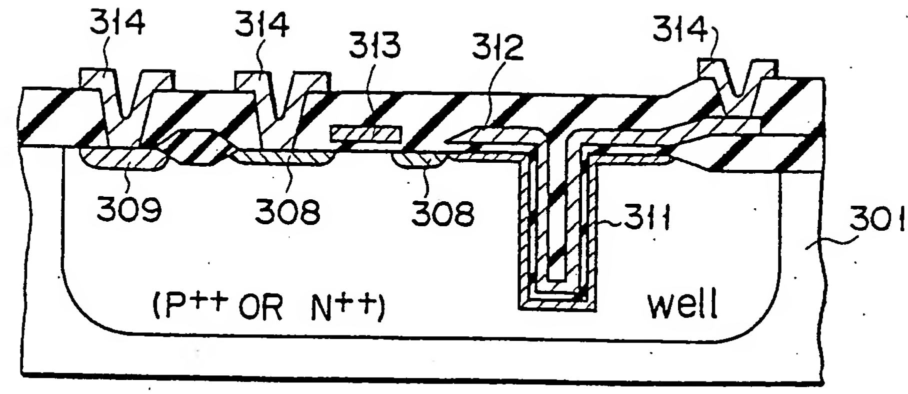


FIG. 10

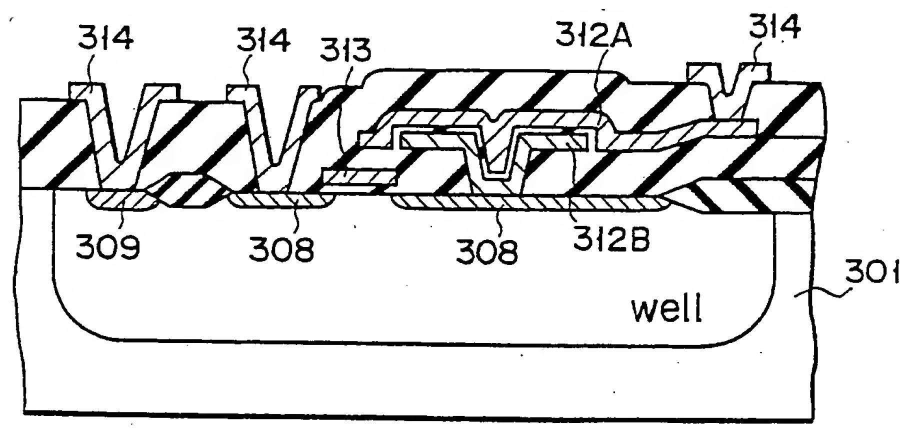


FIG. 11

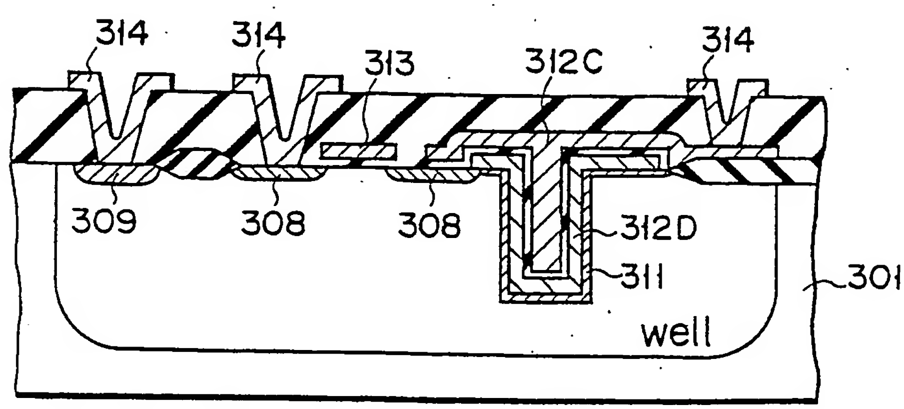


FIG. 12

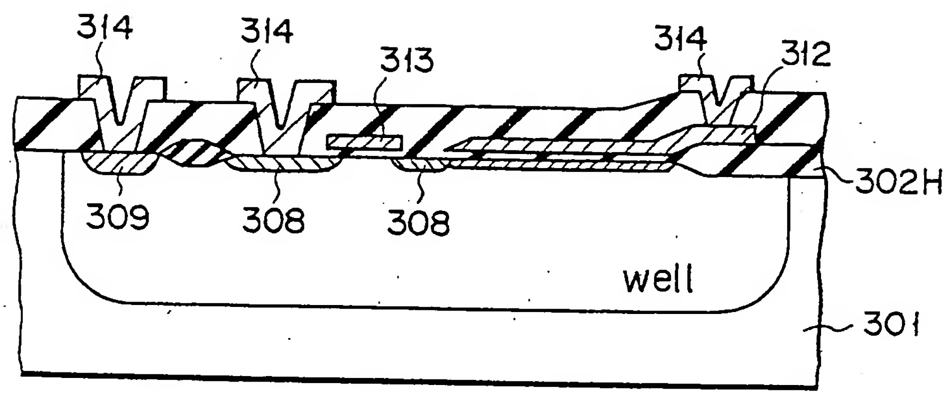

314
314
313
314
312
302H
309
308
308
well
301

FIG. 13

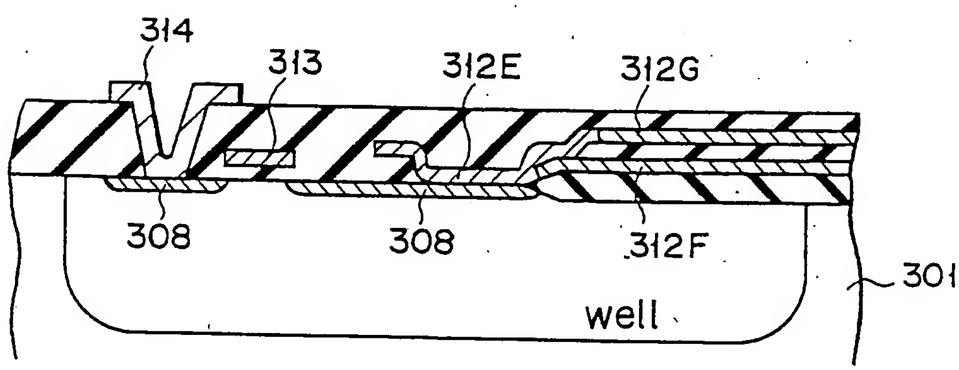

314
313
312E
312G
308
308
312F
301
well

FIG. 14

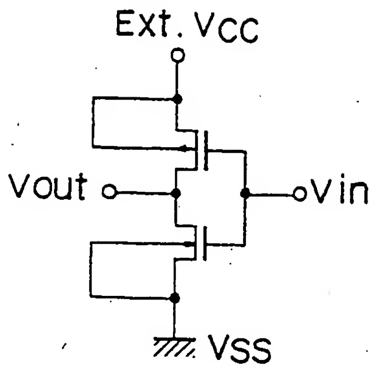


FIG. 15A

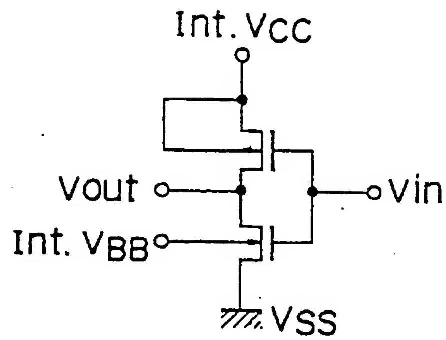


FIG. 15B

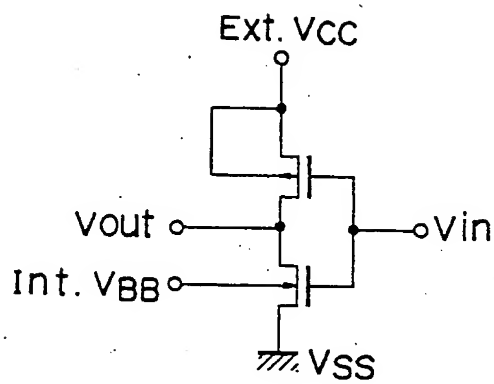


FIG. 15C

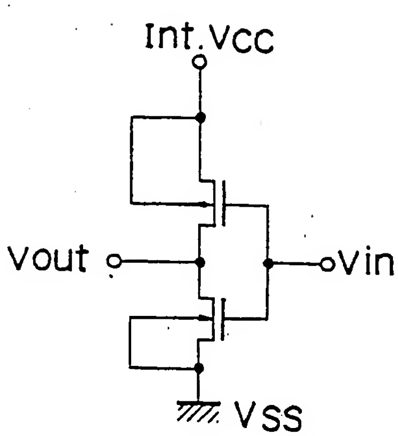


FIG. 15D

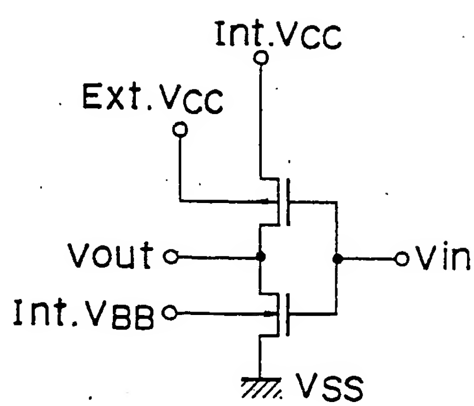


FIG. 15E